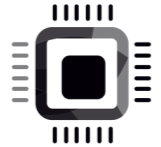
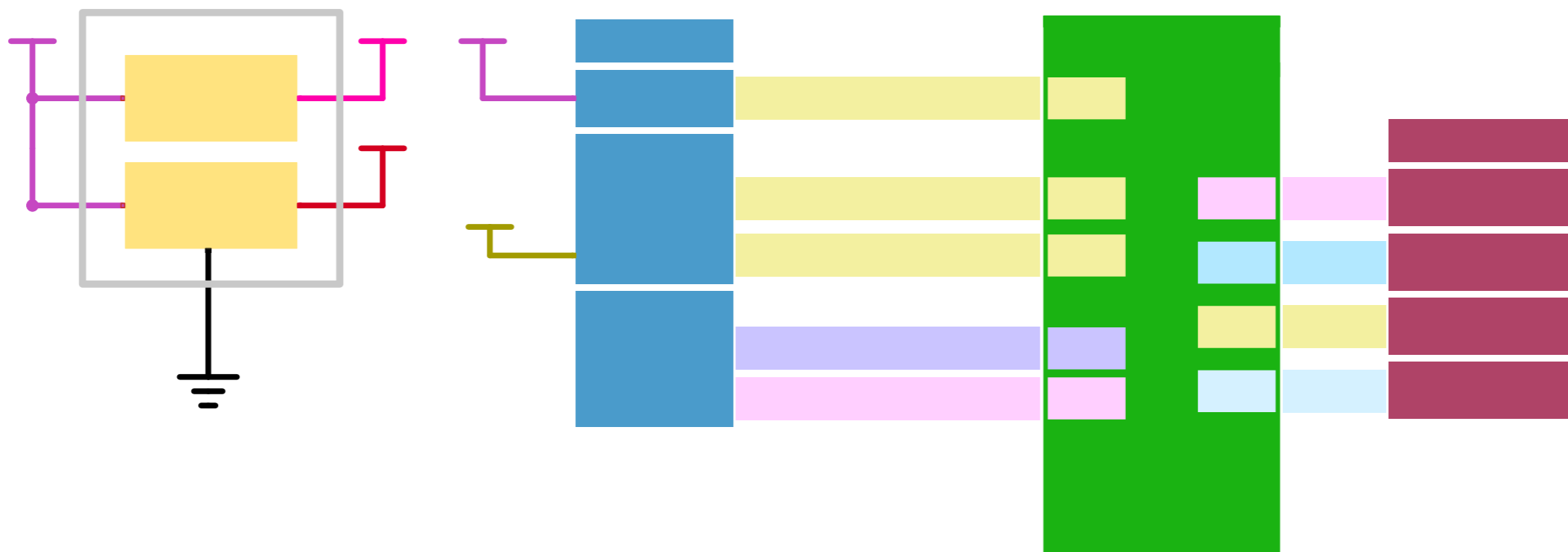
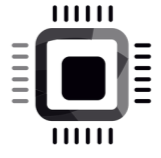
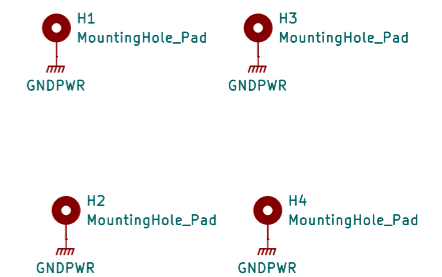
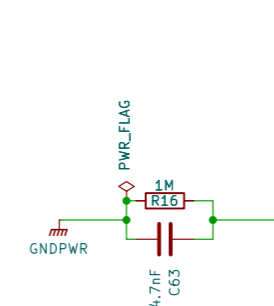
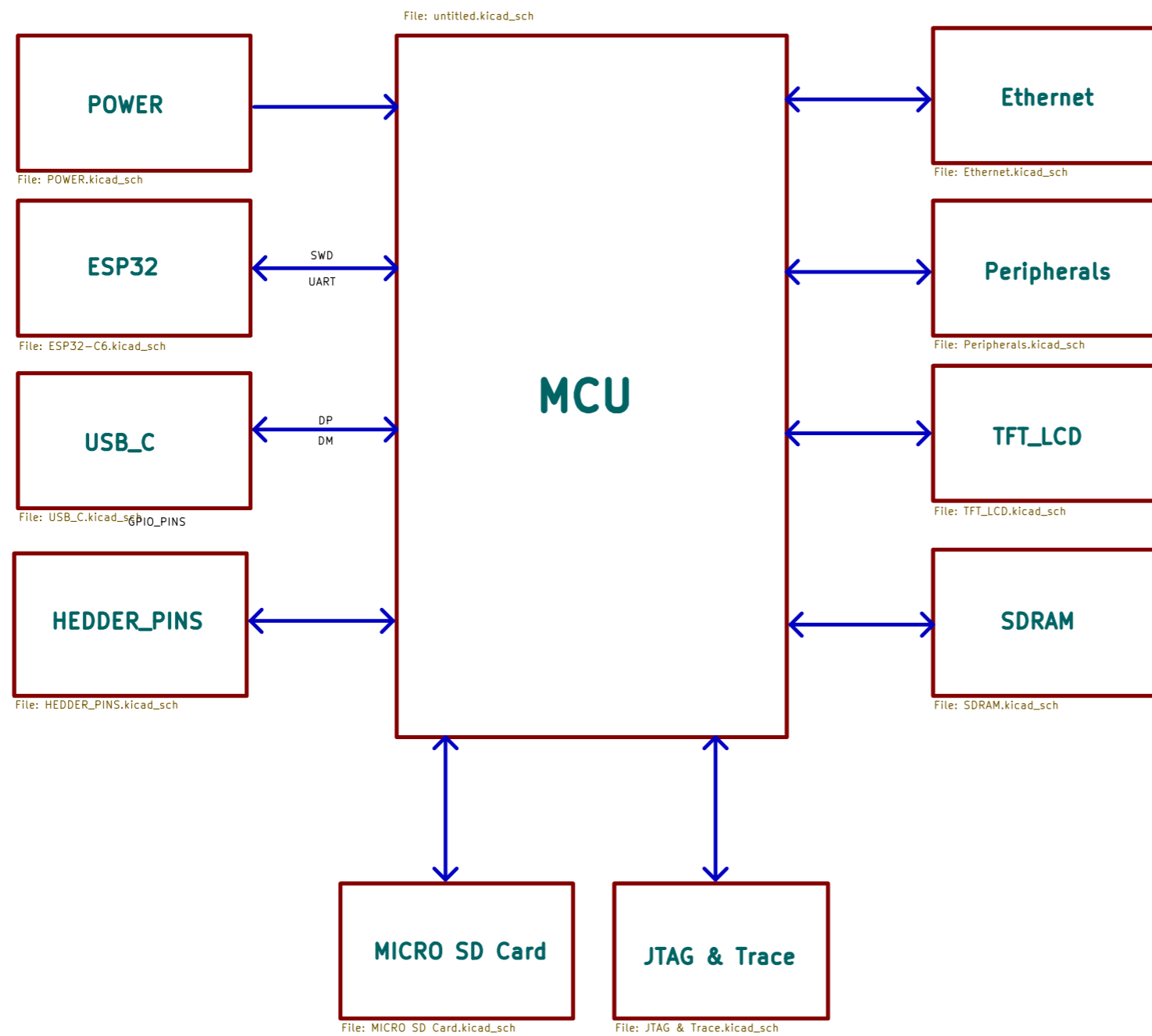



<b>FASTBIT EMBEDDED TECHNOLOGIES PVT LTD</b>	
Project	<<PROJECT TITLE HERE>>
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	Version <b>rev_a1</b>
	Date <<YYYY-MM-DD>>
	Sheet 1 / 14
Notes <<SHORT NOTE>>	

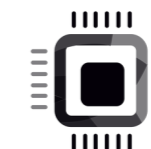


FASTBIT EMBEDDED TECHNOLOGIES PVT LTD	
Project	<<PROJECT TITLE HERE>>
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	Version <b>rev_a1</b>
	Date <<YYYY-MM-DD>>
	Sheet 2 / 14
Notes <<SHORT NOTE>>	

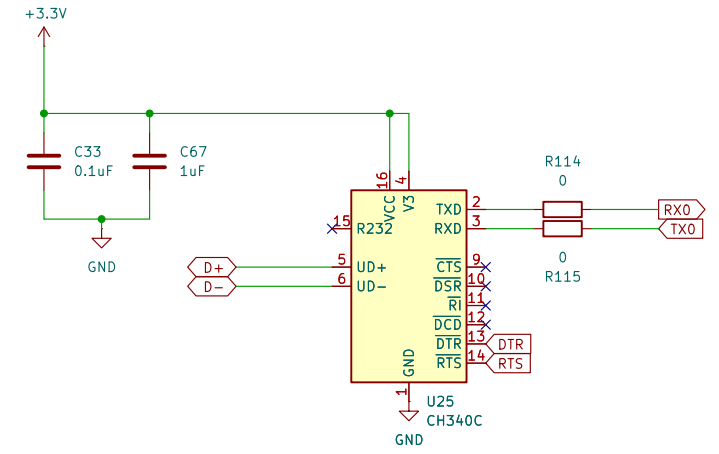
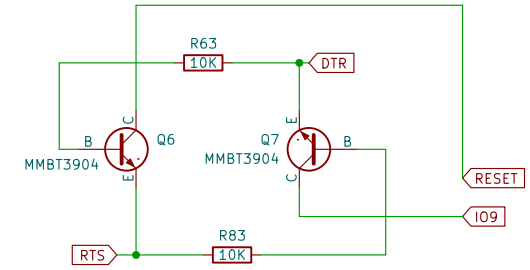
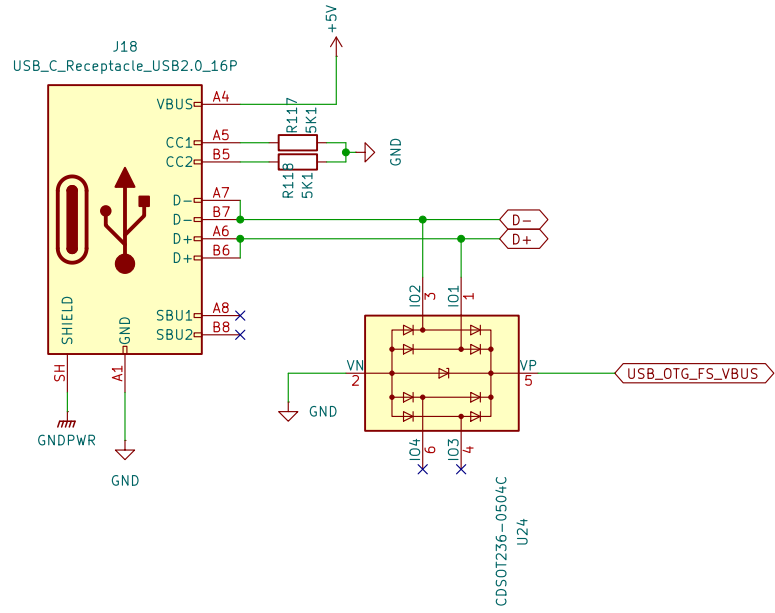
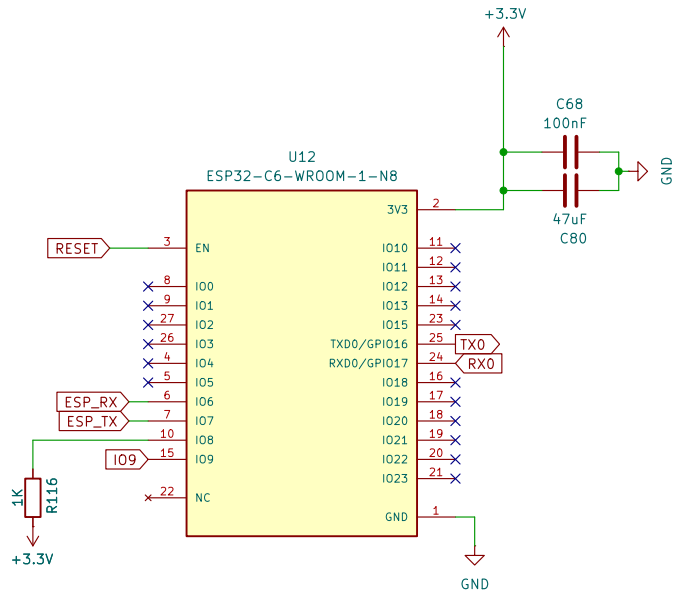


## FASTBIT EMBEDDED TECHNOLOGIES PVT LTD

Project <<PROJECT TITLE HERE>>

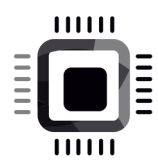


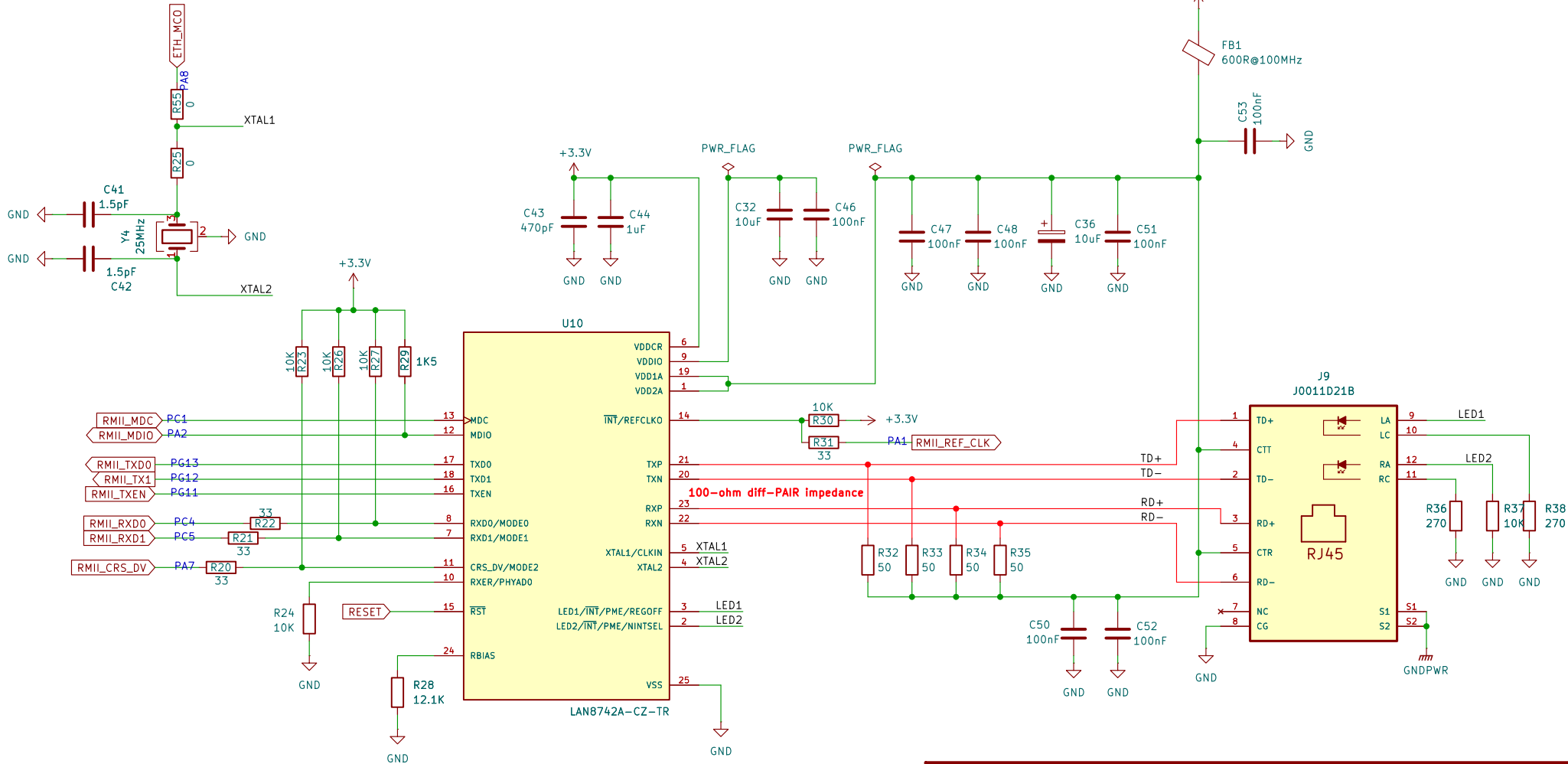
Client	<<CLIENT NAME>>
Developer 1	<<LEAD ENGINEER NAME>>
Developer 2	<<SECOND ENGINEER NAME>>
Reviewer	<<REVIEWER NAME>>
Version	rev_a1
Date	<<YYYY-MM-DD>>
Sheet	3 / 14
Notes	<<SHORT NOTE>>



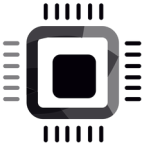
## FASTBIT EMBEDDED TECHNOLOGIES PVT LTD

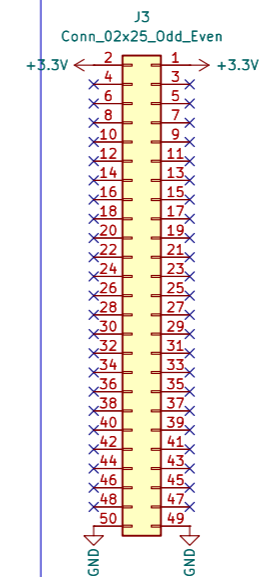
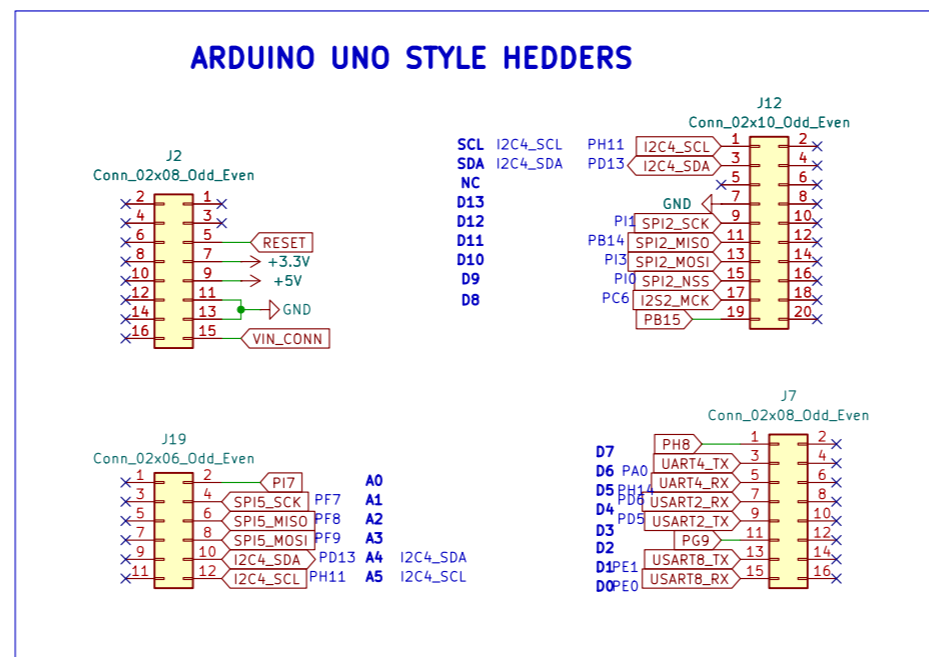
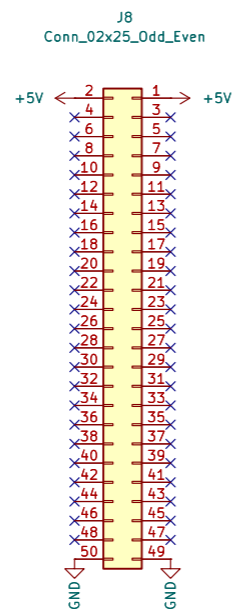
Project <<PROJECT TITLE HERE>>

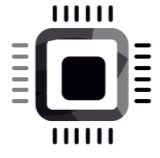
	Client	<<CLIENT NAME>>
	Developer 1	<<LEAD ENGINEER NAME>>
	Developer 2	<<SECOND ENGINEER NAME>>
	Reviewer	<<REVIEWER NAME>>
	<b>Version</b>	<b>rev_a1</b>
	Date	<<YYYY-MM-DD>>
	Sheet	4 / 14
Notes	<<SHORT NOTE>>	



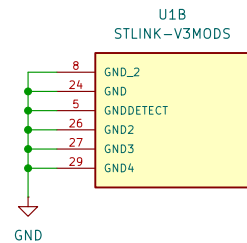
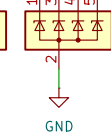
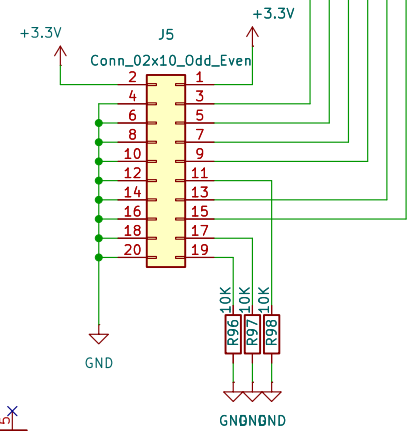
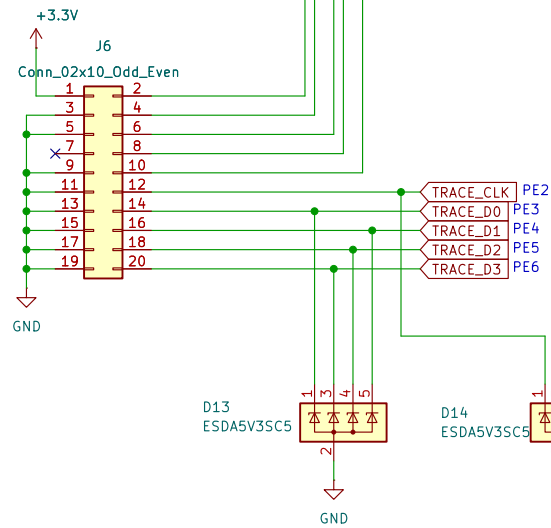
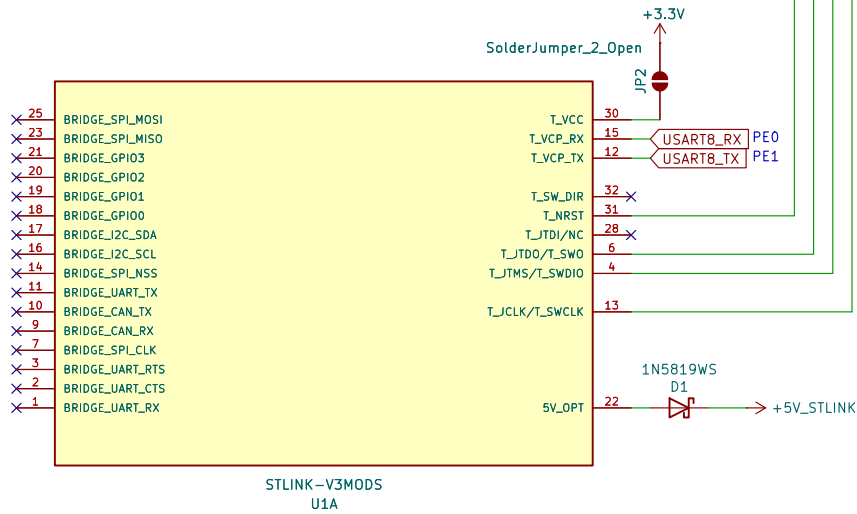
- ◆ It is a **routing standard** (the way wires are organized), not a single physical part.
- **What it stands for: RMII = Reduced Media Independent Interface.**
  - **Why it is used:** It is a "shrunk down" wiring plan that uses **fewer pins** (half the wires) to connect the processor to the Ethernet chip. This saves space on the circuit board while keeping the connection fast.

<b>FASTBIT EMBEDDED TECHNOLOGIES PVT LTD</b>	
Project <<PROJECT TITLE HERE>>	
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	<b>Version</b> <b>rev_a1</b>
	Date <<YYYY-MM-DD>>
	Sheet 5 / 14
Notes <<SHORT NOTE>>	



FASTBIT EMBEDDED TECHNOLOGIES PVT LTD	
Project	<<PROJECT TITLE HERE>>
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	Version <b>rev_a1</b>
	Date <<YYYY-MM-DD>>
	Sheet 6 / 14
Notes <<SHORT NOTE>>	

- PA13 SWDIO R90 22
- PA14 SWCLK R91 22
- PB3 SWO R93 22
- PA15 JTID R92 22
- PB4 TRST R94 22
- RESET R95 22



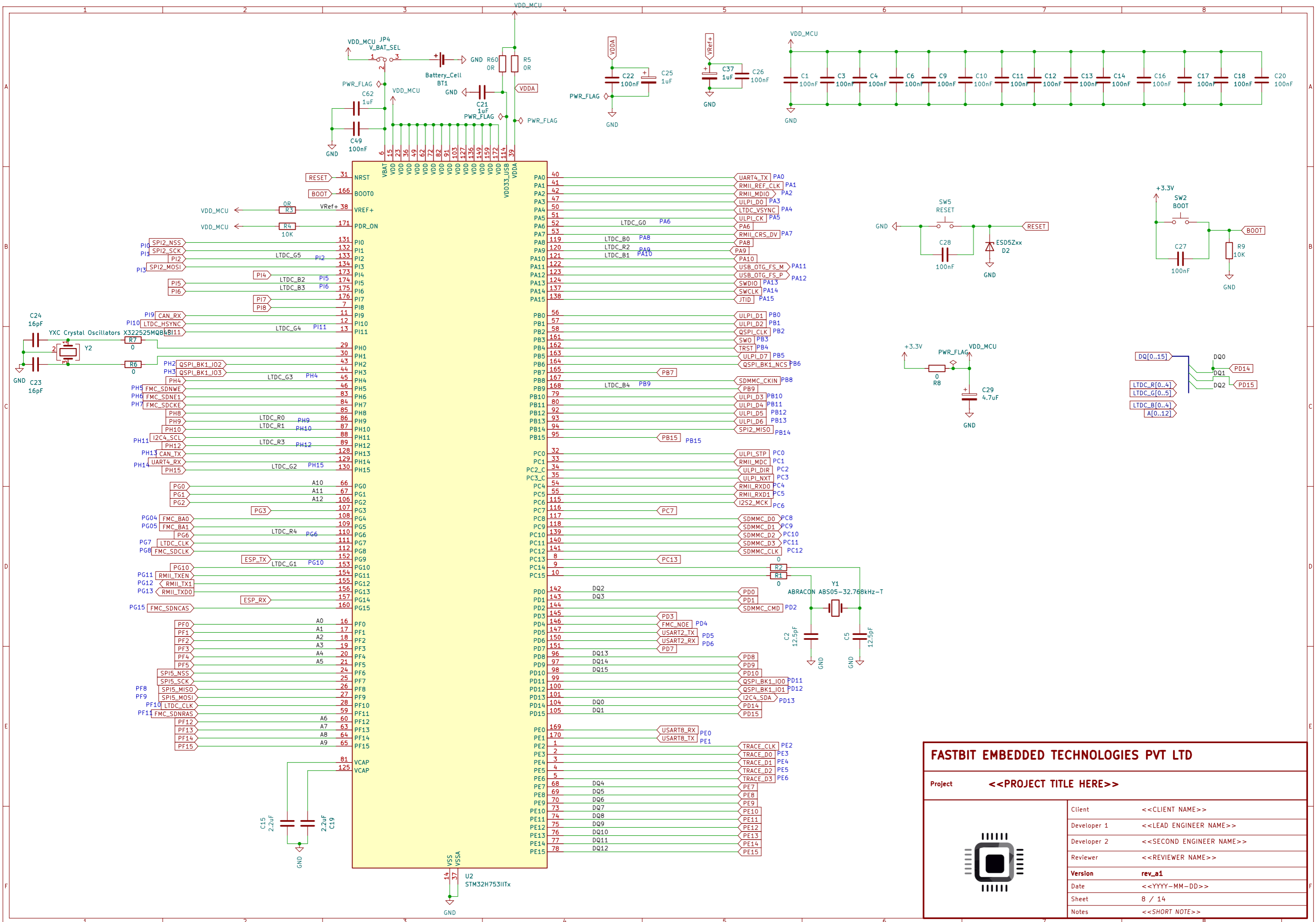
## FASTBIT EMBEDDED TECHNOLOGIES PVT LTD

---

**Project**      <<PROJECT TITLE HERE>>

---


Client	<<CLIENT NAME>>
Developer 1	<<LEAD ENGINEER NAME>>
Developer 2	<<SECOND ENGINEER NAME>>
Reviewer	<<REVIEWER NAME>>
<b>Version</b>	<b>rev_a1</b>
Date	<<YYYY-MM-DD>>
Sheet	7 / 14
Notes	<<SHORT NOTE>>

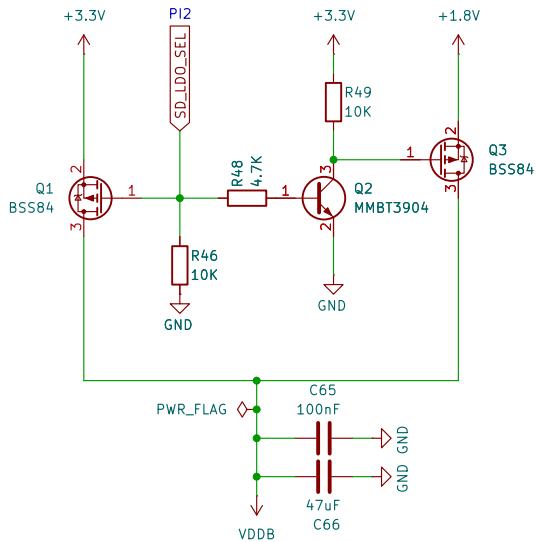
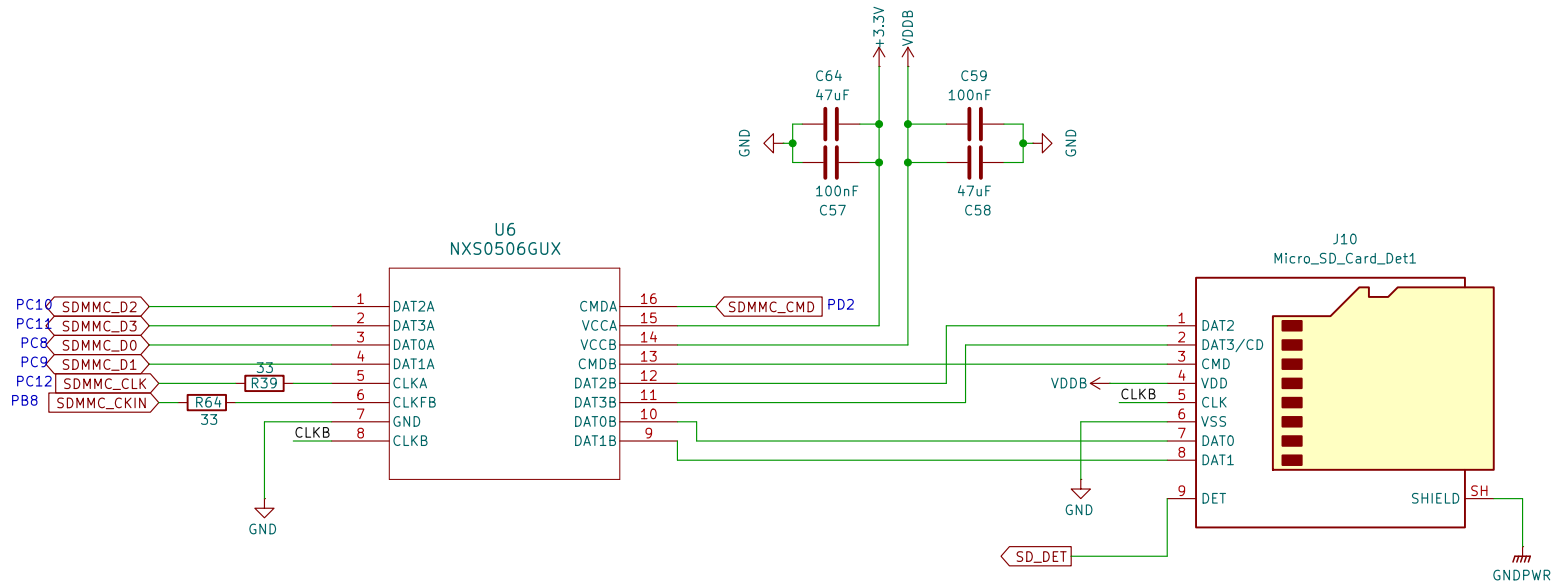


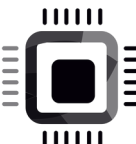
**FASTBIT EMBEDDED TECHNOLOGIES PVT LTD**

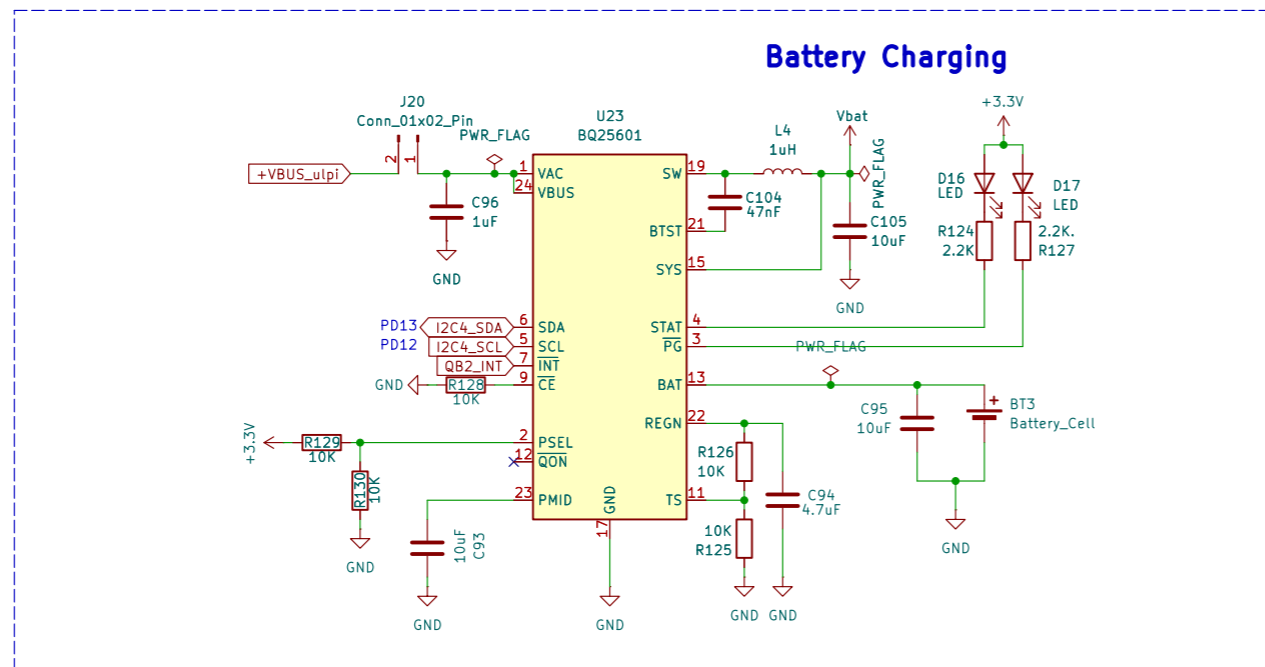
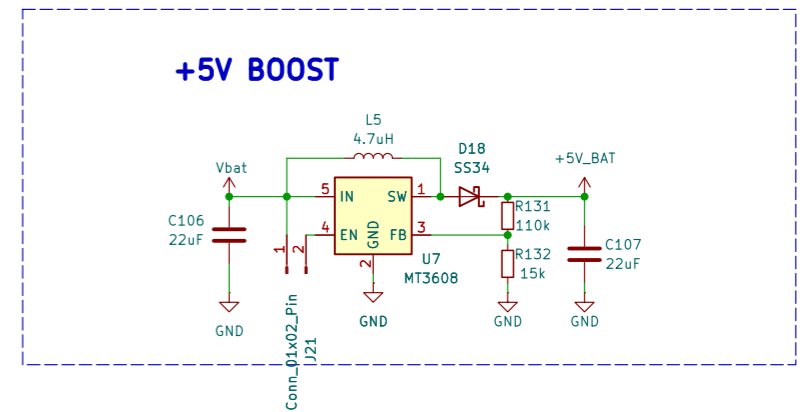
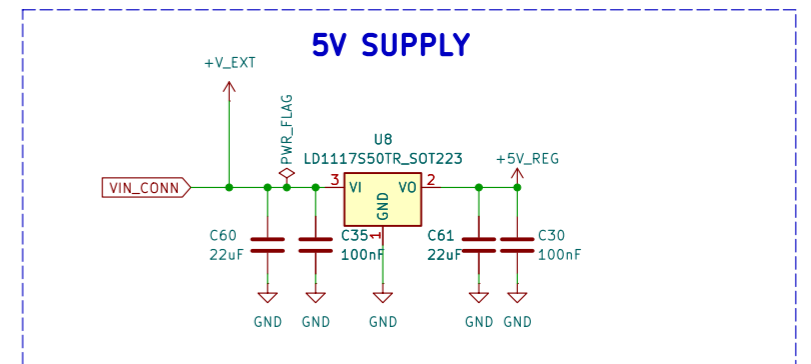
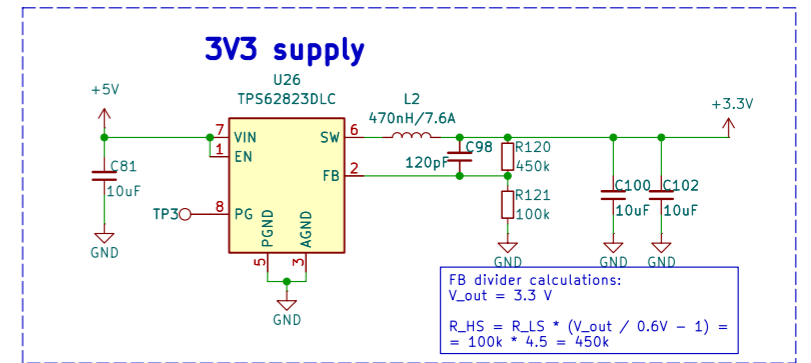
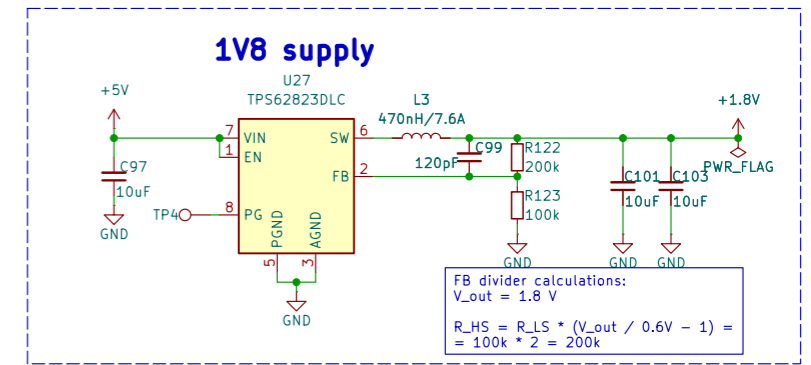
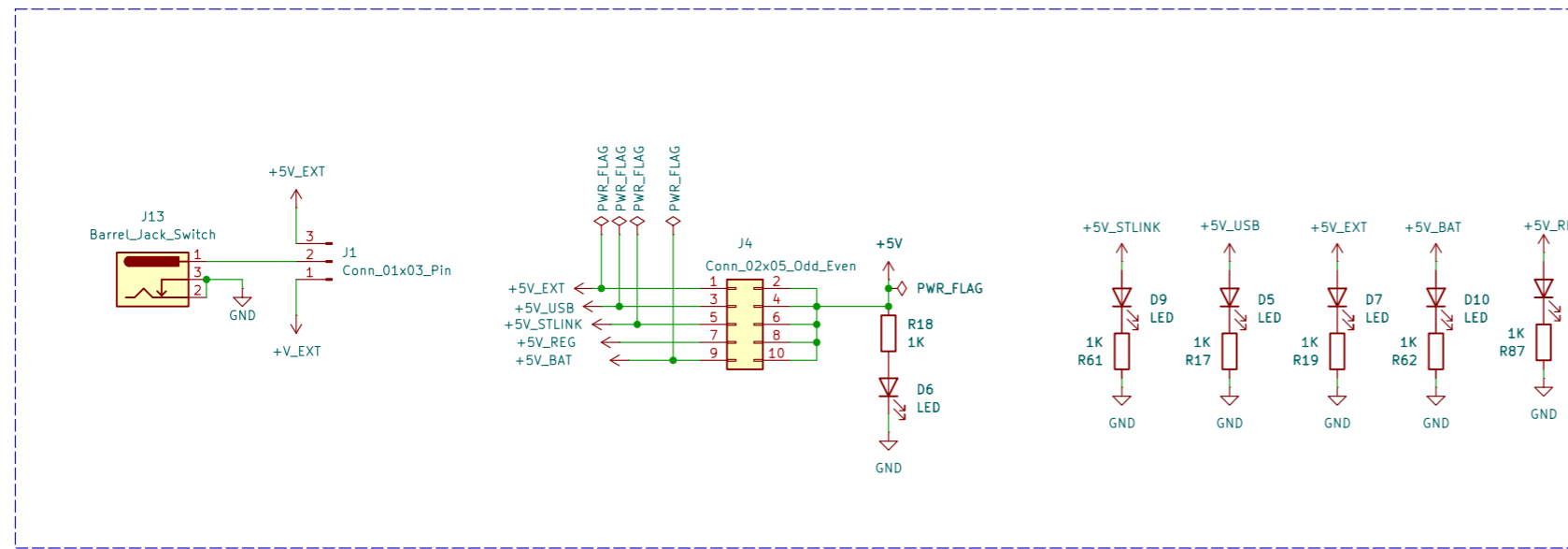
Project <<PROJECT TITLE HERE>>

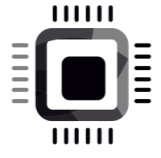
Client	<<CLIENT NAME>>
Developer 1	<<LEAD ENGINEER NAME>>
Developer 2	<<SECOND ENGINEER NAME>>
Reviewer	<<REVIEWER NAME>>
Version	rev_a1
Date	<<YYYY-MM-DD>>
Sheet	8 / 14
Notes	<<SHORT NOTE>>

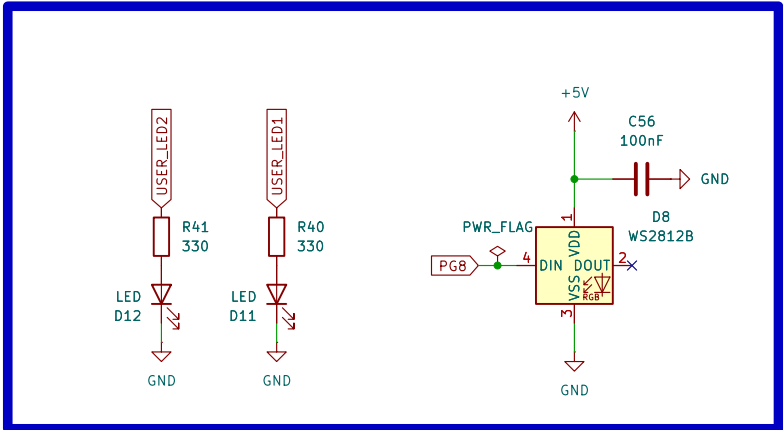
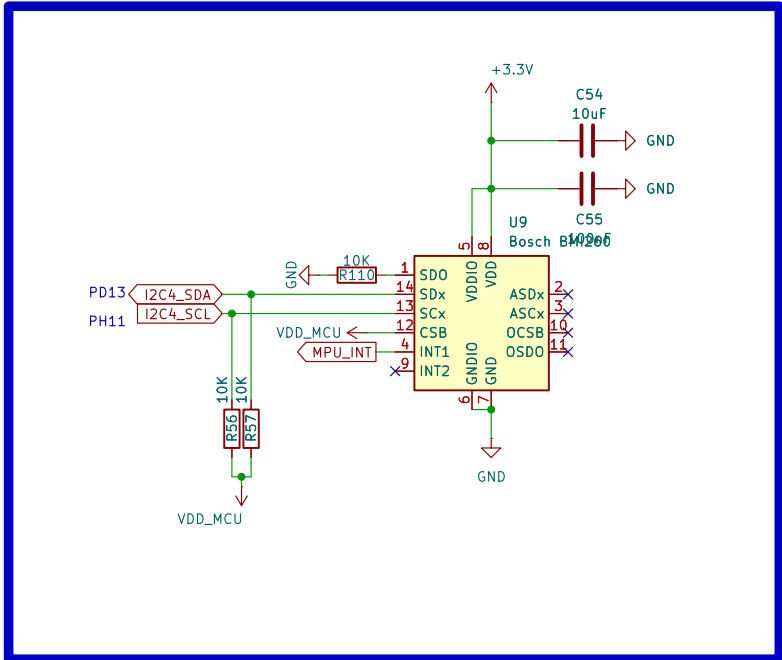
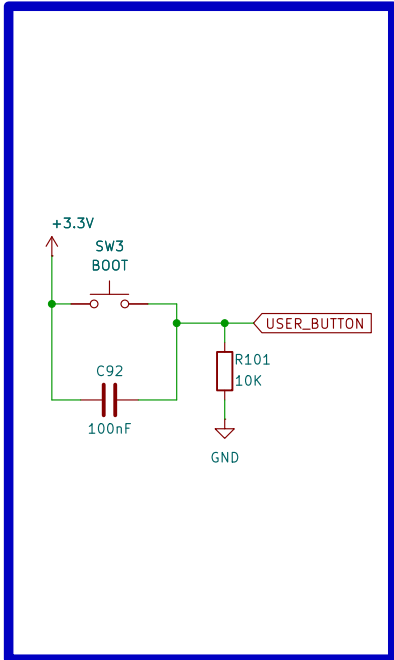
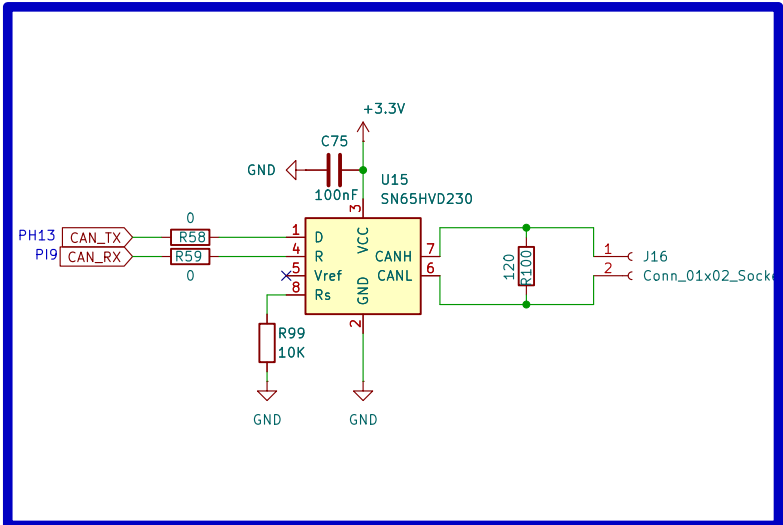
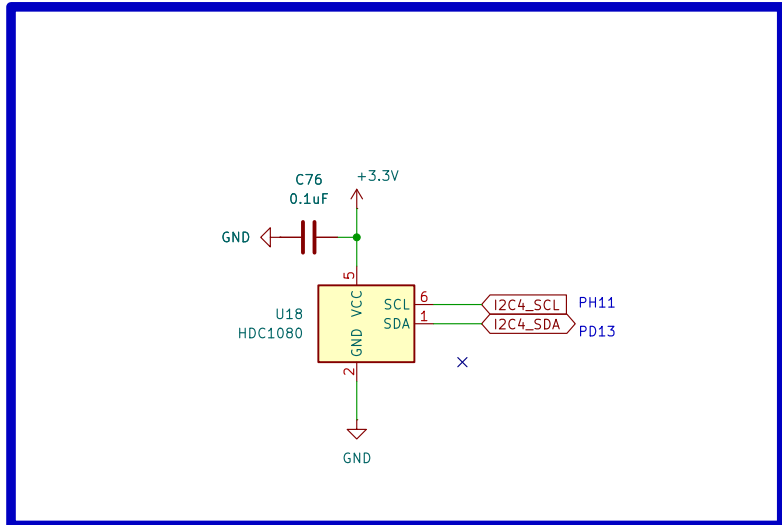
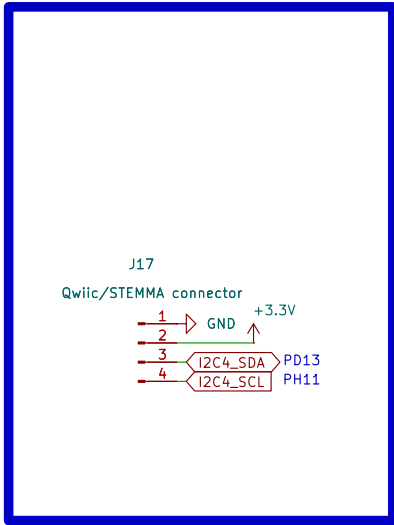




<b>FASTBIT EMBEDDED TECHNOLOGIES PVT LTD</b>	
Project <<PROJECT TITLE HERE>>	
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	<b>Version</b> rev_a1
	Date <<YYYY-MM-DD>>
	Sheet 9 / 14
Notes <<SHORT NOTE>>	

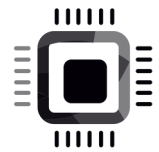


<b>FASTBIT EMBEDDED TECHNOLOGIES PVT LTD</b>	
Project	<<PROJECT TITLE HERE>>
	Client <<CLIENT NAME>>
	Developer 1 <<LEAD ENGINEER NAME>>
	Developer 2 <<SECOND ENGINEER NAME>>
	Reviewer <<REVIEWER NAME>>
	Version <b>rev_a1</b>
	Date <<YYYY-MM-DD>>
	Sheet 10 / 14
Notes <<SHORT NOTE>>	

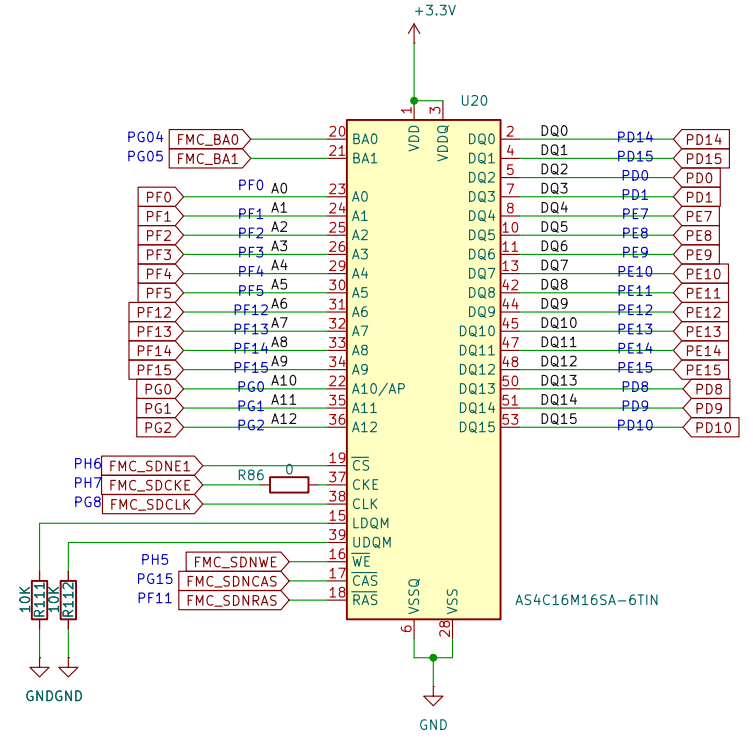
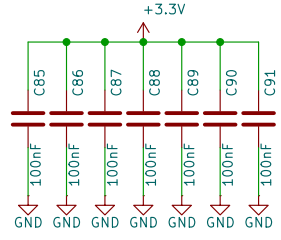
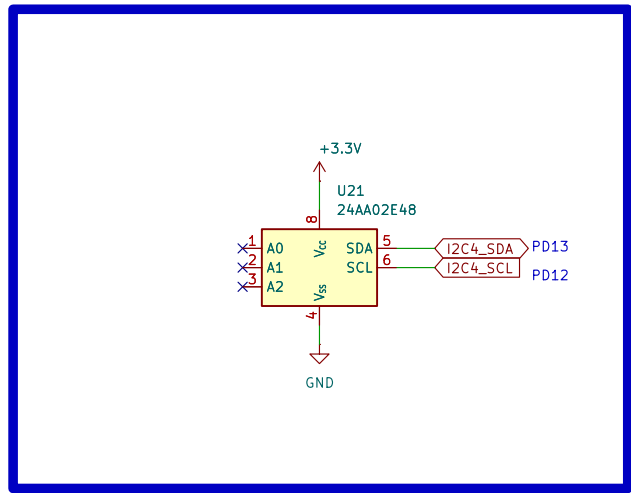
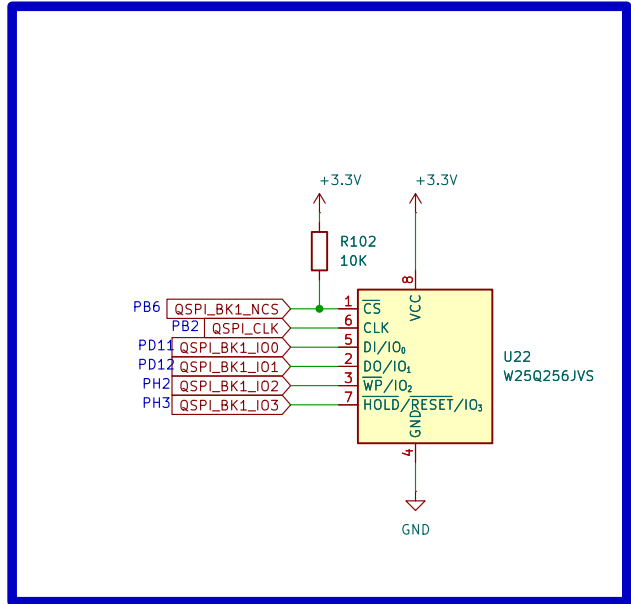


## FASTBIT EMBEDDED TECHNOLOGIES PVT LTD

Project <<PROJECT TITLE HERE>>



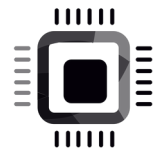
Client	<<CLIENT NAME>>
Developer 1	<<LEAD ENGINEER NAME>>
Developer 2	<<SECOND ENGINEER NAME>>
Reviewer	<<REVIEWER NAME>>
Version	rev_a1
Date	<<YYYY-MM-DD>>
Sheet	11 / 14
Notes	<<SHORT NOTE>>

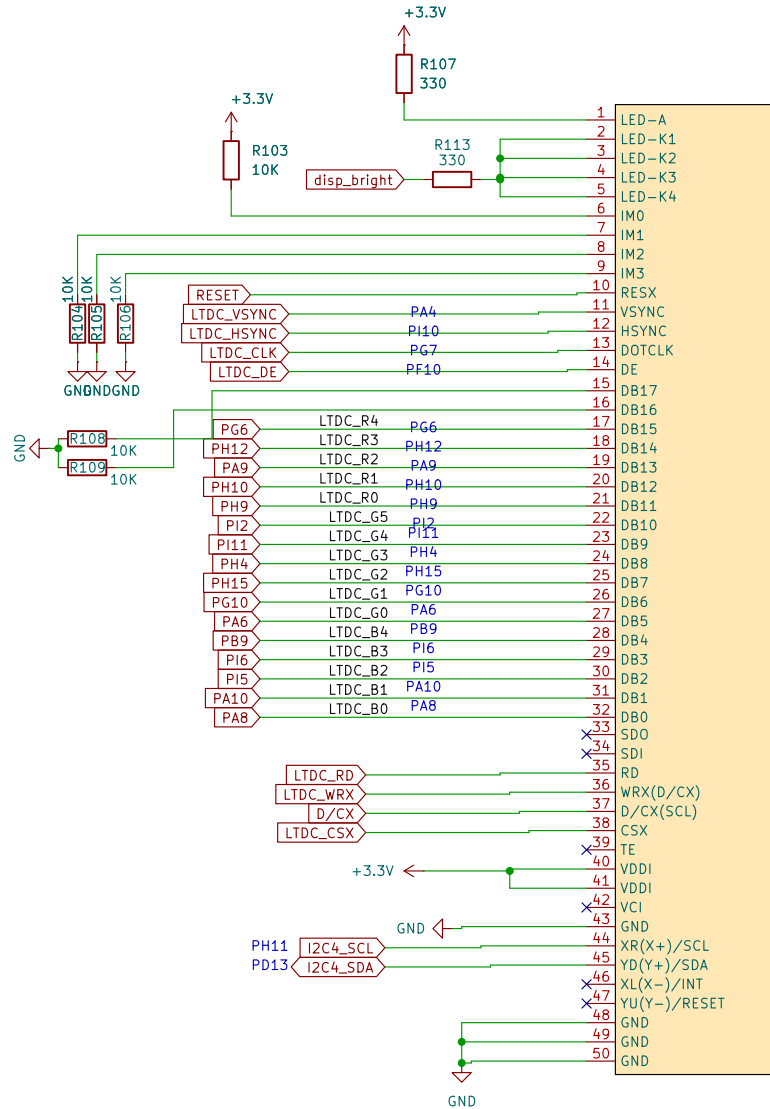


## FASTBIT EMBEDDED TECHNOLOGIES PVT LTD

Project <<PROJECT TITLE HERE>>

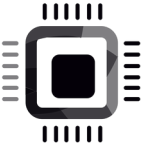
Client	<<CLIENT NAME>>
Developer 1	<<LEAD ENGINEER NAME>>
Developer 2	<<SECOND ENGINEER NAME>>
Reviewer	<<REVIEWER NAME>>
<b>Version</b>	<b>rev_a1</b>
Date	<<YYYY-MM-DD>>
Sheet	12 / 14
Notes	<<SHORT NOTE>>

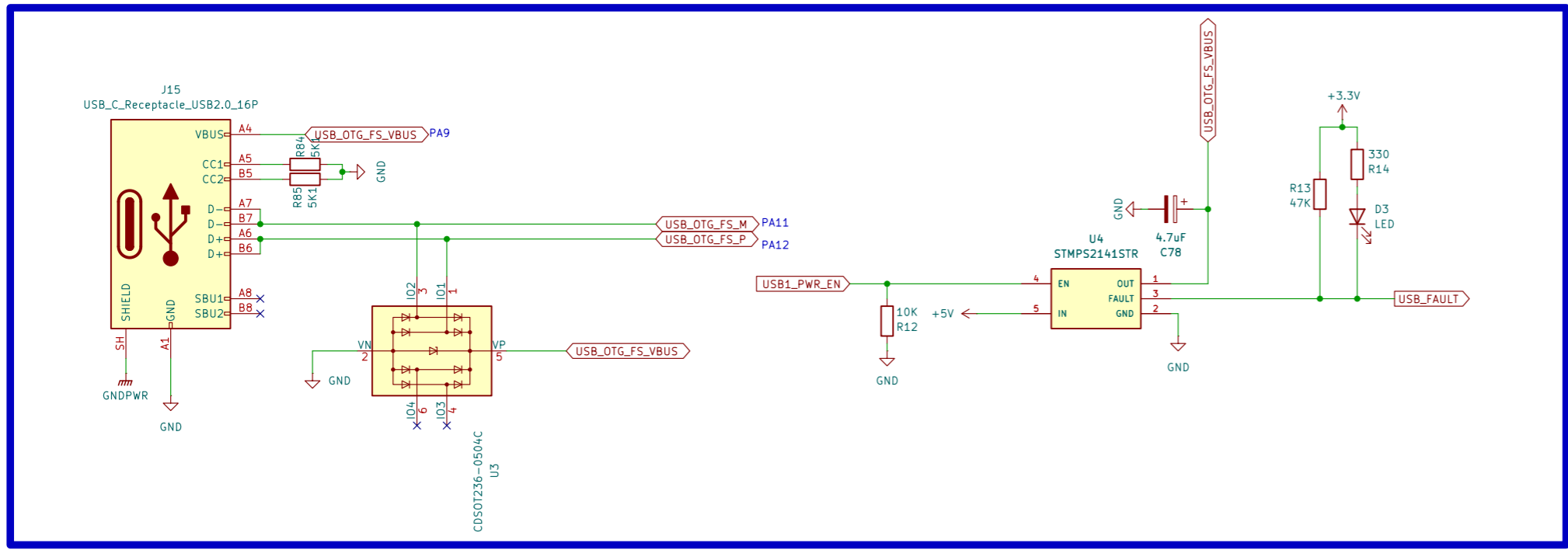
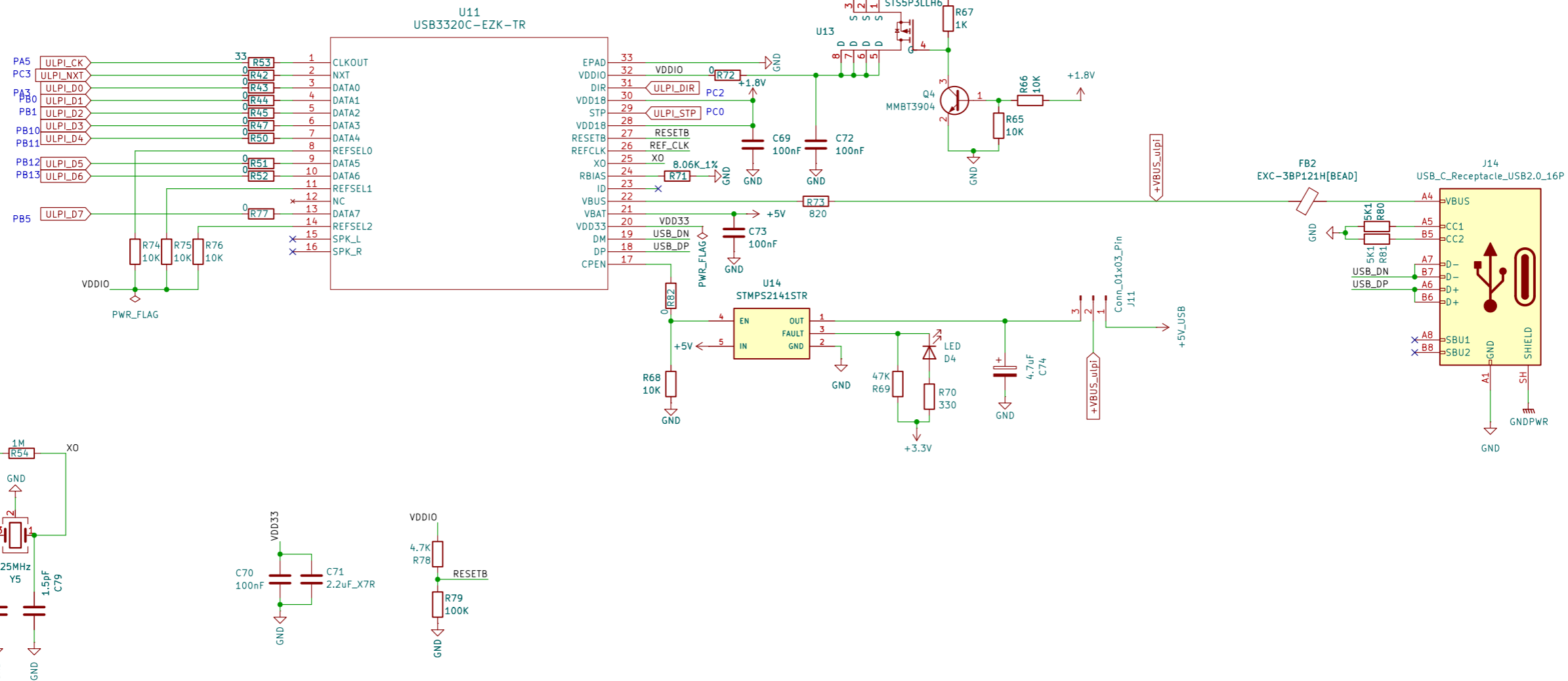


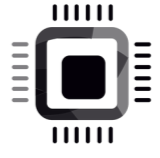


Connector\_FFC-FPC:TE\_5-1734839-0\_1x50-1MP\_P0.5mm\_Horizontal

U5  
tft-connector

FASTBIT EMBEDDED TECHNOLOGIES PVT LTD		
Project	<<PROJECT TITLE HERE>>	
	Client	<<CLIENT NAME>>
	Developer 1	<<LEAD ENGINEER NAME>>
	Developer 2	<<SECOND ENGINEER NAME>>
	Reviewer	<<REVIEWER NAME>>
	Version	rev_a1
	Date	<<YYYY-MM-DD>>
	Sheet	13 / 14
Notes	<<SHORT NOTE>>	



FASTBIT EMBEDDED TECHNOLOGIES PVT LTD		
Project	<<PROJECT TITLE HERE>>	
	Client	<<CLIENT NAME>>
	Developer 1	<<LEAD ENGINEER NAME>>
	Developer 2	<<SECOND ENGINEER NAME>>
	Reviewer	<<REVIEWER NAME>>
	Version	rev_a1
	Date	<<YYYY-MM-DD>>
	Sheet	14 / 14
Notes	<<SHORT NOTE>>	